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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,874	08/06/2001	Robert Chang	SNDK.254US0	9759

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,874	CHANG ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-35* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed November 18, 2004 in response to PTO Office Action mailed May 18, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1 and 31 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-35 are now pending in this application.

3. The objection to claims 1 and 31 has been withdrawn due to the amendment filed November 18, 2004.

Response to Arguments

4. Applicant's arguments, see Remarks, filed November 18, 2004, with respect to the rejection(s)of claim(s) 1and 31 under 35 USC 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Klein (US6,216,224) and Bealkowski (US 5,410,699).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5-9, 14, 16-19, 22-23, 26-27, 29, 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) and Bealkowski (US5,410,699).

As per claim 1, Klein discloses a system for starting operation of an intelligent device comprising: an application and file storage device configured to read and write data files [*firmware routines are transferred from a ROM which may be programmable*; col. 1, lines 13-18], one or more of the data files including the basic input/output system (BIOS) interface [*firmware routines include BIOS*; col. 1, lines 28-32]; random access memory (RAM) [*RAM 118*, Figs. 1 and 2]; a loading logic circuit that copies a portion of the BIOS from the storage device into the RAM [*firmware routine from the ROM address is transferred to corresponding RAM address by RSC*; col. 3, line 61 - col. 4, line 9].

However, Klein does not specifically teach an application and file storage device, such as a solid-state memory, magnetic or optical memory as described in applicant's specification.

Bealkowski discloses loading a BIOS image from a DASD to RAM to directly load BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6). Since the technology for implementing the loading of BIOS from a DASD to RAM was well known as evidenced by Bealkowski,

an artisan would have been motivated to implement this feature in the system of Klein. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Klein to include loading a BIOS from an application and file storage device to RAM because it was well known to benefit by directly loading BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6) as taught by Bealkowski.

As per claim 2, Klein discloses the loading logic circuit is configured to copy the portion of the BIOS from the application and file storage device into the RAM without using a microprocessor [*system controller 114 is driven by RSC 202 rather than by CPU 106*; Fig. 2; col. 4, lines 3-46].

As per claim 5, Klein discloses the loading logic circuit is contained in a field programmable gate array (FPGA) [*RSC may be implemented in a programmable logic array*; col. 8, lines 63 - col. 9, line 1].

As per claim 6, Klein discloses that the loading logic circuit is contained in a programmable logic device [*RSC may be implemented in a programmable logic array*; col. 8, line 63 - col. 9, line 1].

As per claim 7, Klein discloses the circuit comprises board level components [*RSC may be implemented as application specific integrated circuitry or as hardwired logic circuitry*; col. 8, lines 63-67].

As per claim 8, Klein discloses the loading logic circuitry stores the BIOS at any location of the storage device [col. 8, lines 54-62; col. 9, lines 33-37].

As per claim 9, Klein discloses the loading logic circuitry copies the BIOS to any location in the RAM [col. 8, lines 54-62; col. 9, lines 33-37].

As per claim 14, Klein discloses a method of starting a smart device comprising: resetting operation of a microprocessor [*CPU is held in a reset state*; col. 4, lines 8-9]; and thereafter suspending operation of the microprocessor [*CPU is released after transfer of firmware routines is completed*; *thus, CPU was on hold during transfer*; col. 4, lines 9-10]; and thereafter copying a portion of a BIOS from an application and file storage device into RAM [*firmware routines are transferred from Tom to RAM*; col. 4, lines 7-9]; and thereafter starting operation of the microprocessor [*CPU begins to fetch and executes instruction*; col. 4, lines 7-17].

However, Klein does not specifically teach an application and file storage device, such as a solid-state memory, magnetic or optical memory as described in applicant's specification.

Bealkowski discloses loading a BIOS image from a DASD to RAM to directly load BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6). Since the technology for implementing the loading of BIOS from a DASD to RAM was well known as evidenced by Bealkowski,

an artisan would have been motivated to implement this feature in the system of Klein. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Klein to include loading a BIOS from an application and file storage device to RAM because it was well known to benefit by directly loading BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6) as taught by Bealkowski.

As per claim 16, Klein discloses further comprising the step of reading the portion of the BIOS from the RAM with the central processing unit after the step of starting operation of the microprocessor [col. 4, lines 10-13].

As per claim 17, Klein discloses the step of copying the BIOS from a memory storage device into RAM is controlled by a state machine [*state machine transfers firmware routines from ROM to RAM*; col. 4, lines 7-8].

As per claim 18, Klein discloses the state machine is implemented in an ASIC [col. 8, lines 65-66].

As per claim 19, Klein discloses the state machine is implemented in an FPGA [*RSC may be implemented in a programmable logic array*; col. 8, lines 63 - col. 9, line 1].

As per claim 22, Klein discloses a method of providing an interface between an operating system and hardware devices comprising: storing the interface in an application and file storage device [*firmware routines are transferred from a ROM which may be programmable*; col. 1, lines 13-18]; and thereafter copying the interface from the application and application and file storage device into RAM without using a microprocessor [*system controller 114 is driven by RSC 202 rather than by CPU 106*; Fig. 2; col. 4, lines 3-46].

However, Klein does not specifically teach an application and file storage device, such as a solid-state memory, magnetic or optical memory as described in applicant's specification.

Bealkowski discloses loading a BIOS image from a DASD to RAM to directly load BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6). Since the technology for implementing the loading of BIOS from a DASD to RAM was well known as evidenced by Bealkowski, an artisan would have been motivated to implement this feature in the system of Klein. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Klein to include loading a BIOS from an application and file storage device to RAM because it was well known to benefit by directly loading BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6) as taught by Bealkowski.

As per claim 23, Klein discloses the interface is a basic input output system (BIOS) of routines [*firmware routines include BIOS*; col. 1, lines 28-32].

As per claim 26, Klein discloses the step of copying the interface is controlled by a logic loading circuit [*firmware routine from the ROM address is transferred to corresponding RAM address by RSC*; col. 3, line 61 - col. 4, line 9].

As per claim 27, Klein discloses the circuit is implemented on board level components [*RSC may be implemented as application specific integrated circuitry or as hardwired logic circuitry*; col. 8, lines 63-67].

As per claim 29, Klein discloses the step of copying the interface comprises: enabling the application and file storage device and the RAM [*reset 302 starts ROM shadowing operation*; col. 4, line 61 – col. 5, line 4]; and thereafter enabling an address counter to output a value [*initial address in address counter*; col. 5, lines 28-34]; and thereafter correlating the value with a RAM address [*the same address used for ROM and RAM addressing*; col. 5, lines 37-42]; and thereafter sending data from the application and file storage device over a data bus to the RAM address [*the number of clock cycles depends on the intervening buses used*; col. 5, line 28 - col. 6, line 4]; and thereafter incrementing the address counter [*address counter will be incremented as ROM data is transferred*; col. 5, lines 44-47].

As per claim 31, Klein discloses a system for booting a microprocessor controlled device comprising: an application and file storage device having a plurality of files [*firmware routines are transferred from a ROM which may be programmable*; col. 1, lines 13-18]; random access memory [*RAM 118*, Figs. 1 and 2]; a microprocessor [*CPU 106*; Figs. 1 and 2]; human interface devices [*PC can be used by human operator*; col. 2, lines 13-18]; and an interface for communicating between the microprocessor, the application and file storage device and the human interface devices, the interface residing in a file of the file storage device [*firmware routines in ROM include BIOS*; col. 1, lines 28-32]; and means for copying a portion of the interface into the random access memory without using the microprocessor [*system controller 114 is driven by RSC 202 rather than by CPU 106*; Fig. 2; col. 4, lines 3-46].

However, Klein does not specifically teach an application and file storage device, such as a solid-state memory, magnetic or optical memory as described in applicant's specification.

Bealkowski discloses loading a BIOS image from a DASD to RAM to directly load BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6). Since the technology for implementing the loading of BIOS from a DASD to RAM was well known as evidenced by Bealkowski, an artisan would have been motivated to implement this feature in the system of Klein. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Klein to include loading a BIOS from an application

and file storage device to RAM because it was well known to benefit by directly loading BIOS into the system processor's RAM thereby significantly improving the processing speed of the computer system (col. 7, lines 1-6) as taught by Bealkowski.

As per claim 32, Bealkowski discloses the application and file storage device comprises a non-volatile solid-state memory device [*DASD is non-volatile solid-state memory device*].

7. Claims 3-4, 20-21, 25 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) Bealkowski (US5,410,699) and Christeson et al (US5,579,522).

As per claims 3 and 20, Klein and Bealkowski disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski do not specifically teach that the application and file storage device is a flash memory device as recited in the claim.

Christeson discloses a flash memory as an application and file storage device for storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components (col. 2, lines 36-39). Since the technology for implementing a flash memory was well known and since a flash memory benefits by storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components, an artisan

would have been motivated to use a flash memory in the system of Klein and Bealkowski. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Klein and Bealkowski to include a flash memory storage device because it was well known to benefit by storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components as taught by Christeson.

As per claims 4, 21, 25 and 33, Klein discloses the claimed invention as detailed above in the previous paragraphs. Klein and Bealkowski doe not specifically teach that the application and file storage device is a magnetic or optical disk drive as recited in the claim.

Christeson discloses a magnetic or optical disk drive as an application and file storage device for storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components (col. 4, lines 39-41; col. 2, lines 36-39). Since the technology for implementing a magnetic or optical disk was well known and since a magnetic or optical disk benefits by storing information and instructions without the need for removing and/or replacing any computer system hardware components, an artisan would have been motivated to use a magnetic or optical disk drive in the system of Klein and Bealkowski. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Klein and Bealkowski to include a magnetic or optical disk drive storage device because it was well known to benefit by storing information and instructions

without the need for removing and/or replacing any computer system hardware components as taught by Christeson.

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) Bealkowski (US5,410,699) and Christeson et al (US5,579,522) and further in view of Gefen et al. (US 2002/0138702).

As per claim 24, Klein and Bealkowski and Christeson disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski and Christeson do not specifically teach that the storage device is a NAND flash memory device as recited in the claim.

Gefen discloses a storage device as a NAND flash memory device, which benefits from a lower cost, is non-executable and requires less routing resources (page 1, col. 0008). Since the technology for implementing a NAND flash memory was well known and since a NAND flash memory benefits from a lower cost, is non-executable and requires less routing resources, an artisan would have been motivated to implement a NAND flash in the system of Klein and Bealkowski and Christeson. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Klein and Bealkowski and Christeson to include NAND flash memory device because it was well known to benefit from a lower cost, is non-executable and requires less routing resources as taught by Gefen.

9. Claims 10-11 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) Bealkowski (US5,410,699) and Kim (US5,809,559).

As per claims 10 and 34-35, Klein and Bealkowski disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski does not specifically teach a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten as recited in the claims.

Kim discloses a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten to prevent the BIOS commands from being corrupted (col. 14, lines 65-67). Since the technology for implementing a write protect mechanism in a storage device was well known in the art and since a write protect mechanism benefits by preventing the BIOS commands from being corrupted, an artisan would have been motivated to implement a write protect mechanism in the system of Klein. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Klein and Bealkowski and Kim before him at the time the invention was made, to modify the system of Klein and Bealkowski to include a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten because a write protect mechanism was well known to benefit by preventing the BIOS commands from being corrupted as taught by Kim.

As per claim 11, Klein and Bealkowski disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski do not specifically teach a write protect mechanism generates a first and second write strobe signal for each write strobe signal of a microprocessor as recited in the claim.

Kim discloses a write protect mechanism that generates a first and second write strobe signal for each write strobe signal of a microprocessor to prevent the BIOS commands from being corrupted (col. 14, line 65 - col. 15, line 25). Since the technology for implementing a write protect mechanism generating a first and second write strobe signal for each write strobe signal of a microprocessor was well known in the art and since a write protect mechanism generating a first and second write strobe signal for each write strobe signal of a microprocessor benefits by preventing the BIOS commands from being corrupted, an artisan would have been motivated to implement a write protect mechanism in the system of Klein and Bealkowski. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Klein and Bealkowski and Kim before him at the time the invention was made, to modify the system of Klein to include a write protect mechanism generating a first and second write strobe signal for each write strobe signal of a microprocessor because a write protect mechanism generating a first and second write strobe signal for each write strobe signal of a microprocessor was well known to benefit by preventing the BIOS commands from being corrupted as taught by Kim.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) Bealkowski (US5,410,699) and Cromer et al. (US6,718,464).

As per claim 15, Klein and Bealkowski disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski do not specifically teach a user selecting which BIOS of multiple BIOS to copy into the RAM as recited in the claim.

Cromer discloses a user selecting which BIOS of multiple BIOS to copy into the RAM to customize a client and further specify the configuration of the client computer system (col. 3, lines 27-34). Since the technology for implementing a user selecting which BIOS of multiple BIOS to copy into the RAM was well known and since a user selecting which BIOS of multiple BIOS to copy into the RAM benefits by customizing a client and further specifying the configuration of the client computer system, an artisan would have been motivated to implement a user selecting which BIOS of multiple BIOS to copy into the RAM in the system of Klein and Bealkowski. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Klein and Cromer before him at the time the invention was made, to modify the system of Klein and Bealkowski to include a user selecting which BIOS of multiple BIOS to copy into the RAM because it was well known to benefit by customizing a client and further specifying the configuration of the client computer system as taught by Cromer.

11. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,216,224) Bealkowski (US5,410,699) and Le et al. (US6,154,838).

As per claim 28, Klein and Bealkowski disclose the claimed invention as detailed above in the previous paragraphs. However, Klein and Bealkowski do not specifically teach copying additional interface device commands from the application and file storage device into RAM using the microprocessor as recited in the claim.

Le discloses copying additional interface device commands from the application and file storage device into RAM using the microprocessor to positively affect the economics of operating and maintaining the computer system (col. 14, lines 24-39). Since the technology for implementing the copying of additional interface device commands from the application and file storage device into RAM using the microprocessor was well known and since copying additional interface device commands from the application and file storage device into RAM using the microprocessor benefits by positively affect the economics of operating and maintaining the computer system, an artisan would have been motivated to implement the copying of additional interface device commands from the application and file storage device into RAM using the microprocessor in the system of Le. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Klein and Bealkowski and Le before him at the time the invention was made, to modify the system of Klein and Bealkowski to include copying of additional interface device commands from the application and file storage device into RAM using the microprocessor because it was

well known to positively affect the economics of operating and maintaining the computer system as taught by Le.

As per claim 30, Klein discloses the claimed invention as detailed above in the previous paragraphs. However, Klein does not specifically teach using error correction code as recited in the claim.

Le discloses using error correction code to positively affect the economics of operating and maintaining the computer system (col. 14, lines 24-39). Since the technology for implementing error correction code was well known and since an error correction code benefits by positively affecting the economics of operating and maintaining the computer system, an artisan would have been motivated to implement an error correction code in the system of Le. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Klein and Bealkowski and Le before him at the time the invention was made, to modify the system of Klein and Bealkowski to include an error correction code because it was well known to positively affect the economics of operating and maintaining the computer system as taught by Le.

Allowable Subject Matter

12. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

As per claim 12, the prior art of record does not teach or suggest a first write strobe signal separated from a second write strobe SIGNAL by a period of time, and wherein the first write strobe signal records the location of the BIOS in the storage device and the command code to the storage device, and the second write strobe signal enables writing of the storage device in combination with the other elements set forth in the claimed invention.

Therefore, dependent claim 13 is allowable as being dependent upon claim 12 and having additional allowable features therein.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach copying BIOS from application and file storage device into RAM without using a microprocessor and write protect a location having BIOS from overwrite.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 18, 2005

Pierre M. Vital
Primary Examiner
Art Unit 2188